



SystemVerilog@DAC

Accellera's SystemVerilog Workshop

Monday, June 2, 2003

9:00am

Room 304AB, Anaheim Convention Center

This workshop will provide details of the SystemVerilog language, syntax and semantics presented by experts. In addition, leading-edge designers and verification users from Intel, Infineon, and Verification Central will share their experiences.

Accellera / Axis Breakfast and Panel Discussion: When is Verification Really Done?

Co-Sponsored by Axis Systems

Marriott Anaheim Hotel, Marquis Ballroom

Wednesday, June 4, 2003

7:30am - 9:00am

Anaheim, CA

Considering that you can spend up to 70% of your entire design process on verification, the answer to the question, "When is verification really done?" will undoubtedly affect your productivity, product quality and "time to market."

What are the metrics critical to achieving the best results? What are the advantages of new methodologies based on the new Accellera standards? Since the gap is steadily increasing between what can be designed versus what can be verified, can these questions even be answered?

This panel will examine methods, metrics, and guidelines that produce system verification closure. End users and tool developers will present their experiences with different verification processes and toolsets, illuminating both their advantages and their drawbacks. Additionally, methods to boost verification productivity and metrics to measure verification completeness will be discussed. Lastly, end users and tool developers will share their future visions for verification and will explain the role of Accellera standards in boosting verification productivity and closing the verification gap.

Synopsys Interoperability Breakfast: Discover the Hidden Technology Behind Nanometer Design - What Successful Companies Are Doing

Sponsored by IBM

Moderator: Chi-Foon Chan

Panelist: Raul Camposano

Wednesday, June 4, 2003

7:30am - 9:30am

Pacific Ballroom B, Hilton Anaheim Hotel

Accellera Open Membership Meeting

Wednesday, June 4, 2003

10:00am - 11:30am

Room 212B, Anaheim Convention Center

Please join us for an update and outlook on Accellera technical activities, including presentations on Verilog-AMS, Standard Co-Emulation Application Modeling Interface (SCE-MI), PSL, OVL, VHPI and SystemVerilog.

Accellera Designer's Forum - Open Membership Meeting

Wednesday, June 4, 2003

11:30am - 12:30pm

Room 212B, Anaheim Convention Center

Tutorial: Assertion-Based Verification

Friday, June 6, 2003

9:00am - 5:00pm

Room 209AB, Anaheim Convention Center

Visit the following companies at DAC for more information on SystemVerilog:

Aldec, Axis, Doulos, @HDL, Interra, Mentor Graphics, Novas, Real Intent, Sunburst Design, Sutherland HDL, SynaptiCAD, Synchronicity, Synopsys, Verplex, Willamette HDL, 0-In

AND, see daily SystemVerilog presentations, delivered by Synopsys, at the Sun and Intel booths.